IN THE SPECIFICATION:

Please **amend** the present specification as set forth below.

Please **replace** the paragraph beginning on page 12, line 3 of the present specification with the following new paragraph:

FIGS. 6A and 6B are a top plan view and a cross-sectional view, respectively, illustrating the formation of a first photoresist pattern 710 as a band-type on a third insulating layer 530 covering the bit line 600 (See FIGS. 5A and 5B). Referring to FIGS. 5A, 5B, 6A and 6B, after forming the bit line 600, a third insulating layer 530 is formed to cover the bit line 600. Preferably, the third insulating layer 530 is a silicon oxide having good gap filling characteristics, e.g., a HDP oxide or a BPSG. Then, the surface of the third insulating layer 530 is planarized as needed. Preferably, the planarizing process is a CMP.

Please **replace** the paragraph beginning on page 13, line 18 of the present specification with the following new paragraph:

Referring to FIGS. 5A, 5B, 7A and 7B, a ~~A~~ band-type opening 531 is obtained by etching along the gate line 200. Thus, the plurality of first contact pads 410 are exposed in rows within the region exposed by the band-type opening 531. Also, the band-type opening 531 is formed across the bit lines 600 which are adjacent to the first contact pads 410. As illustrated in FIGS. 7B and 5B, since the sides and the tops of the bit lines 600 are prevented from being damaged during the etching process by the bit line spacer 670 and the bit line capping insulating layer 660, the bit lines 600 are not exposed by the band-type opening 531.

Please **replace** the paragraph beginning on page 14, line 8 of the present specification with the following new paragraph:

FIGS. 8A and 8B are a top plan view and a cross-sectional view, respectively, illustrating the formation of a conductive layer 800 on the third insulating layer 530' to fill the band-type

opening 531. Referring to FIGS. 5A, 5B, 8A and 8B, the conductive layer 800 (e.g., a conductive polysilicon layer), which fills the band-type opening 531, is formed on the patterned third insulating layer 530'. The conductive layer may be thick enough to fill the band-type opening 531 using a CVD process. Preferably, the conductive layer 800, such as a conductive polysilicon layer, extends to cover the third insulating layer 530'. Actually, the conductive layer 800 covers the bit line capping insulating layer 660 and the bit line spacer 670, which cover the bit line 600 and are exposed by the band-type opening 531.

Please **replace** the paragraph beginning on page 15, line 1 of the present specification with the following new paragraph:

Referring to FIGS. 5A, 5B and 9A, because ~~Because~~ portions of the storage electrode contact bodies 810 overlap the bit lines 600, an etching process is carried out to expose a top surface of the bit line capping insulating layer 660 formed on the bit line 600 to completely separate the storage electrode contact bodies 810 along the gate lines 200, ~~as illustrated in FIG. 9A~~. Also, when the etching process is performed until the top surface of the third insulating layer 530' is exposed, the separation of the storage electrode contact bodies 810 is completed along the bit lines 600. Because the top surface of the third insulating layer 530' is disposed higher than that of the bit line capping insulating layer 660, the separation process is completed when the top surface of the bit line capping insulating layer 660 is exposed. Preferably, a silicon nitride layer is used to form bit line capping insulating layer 660 and may be used as an etch stopper in the etching process during the separation process.

Please **replace** the paragraph beginning on page 15, line 19 of the present specification with the following new paragraph:

For example, referring to FIGS. 5A, 5B and 9A, the storage electrodes are arranged in zigzag pattern in a direction of the bit lines 600 ~~(See FIG. 9A).~~ In other words, the adjacent storage electrodes are arranged in a diagonal direction from the bit lines 600. In addition, the storage electrodes are arranged to be zigzag pattern in a direction of the gate lines 200. In other words, the adjacent storage electrodes are arranged in a diagonal direction of the gate lines 200. The arrangement of the storage electrodes will be described in more detail with reference to the appended drawings.

Please **replace** the paragraph beginning on page 15, line 27 of the present specification with the following new paragraph:

However, when the storage electrodes are arranged in a diagonal direction of the bit lines 600 (See FIGS. 5A and 5B) or the gate lines 200, the center of the storage electrode may be misaligned from the center of the first contact pad 410. Thus, a top surface of the storage electrode contact body 810 is preferably extended in a direction of the bit line 600 (See FIGS 5A and 5B) to electrically connect the storage electrode with the first contact pad 410.

Please **replace** the paragraph beginning on page 16, line 3 of the present specification with the following new paragraph:

Referring to FIGS. 5A, 5B, 9A and 9B, as ~~As~~ the opening 531 is extended in a direction of the bit line 600 as described above, a body 811, which fills the opening 531 of the storage electrode contact body 810, may be extended in a direction of the bit line 600. Preferably, to increase the contact area between the storage electrode contact body 810 and the storage electrode, the storage electrode contact body 810 has an extension 811 at the top of the body 815. The extension 811 is a portion of the storage electrode contact body 810 that extends over the top of the third insulating layer 530' in a direction toward the bit line 600.

Please **replace** the paragraph beginning on page 16, line 11 of the present specification with the following new paragraph:

Preferably, the second photoresist pattern 750 is used as an etch mask to form the storage electrode contact body 810 having the extension 811. For example, the second photoresist pattern 750 is preferably formed to cover the portion of the conductive layer 800 such that the width of the second photoresist pattern 750 is wider than the opening 531 and forms the extension 811 along a major axis toward a bit line 600. (See FIGS. 5A, 5B, 9A and 9B). In other words, the second photoresist pattern 750 is preferably formed to allow the extension 811 to be extended in a direction of the bit line 600.

Please **replace** the paragraph beginning on page 16, line 19 of the present specification with the following new paragraph:

As illustrated in ~~FIG.~~ FIGS. 5A, 5B, 9A and 9B, the extension 811 of the patterned storage electrode contact body 810 is extended to cover a portion of the top of the third insulating layer 530' and~~, as illustrated in FIG. 9A,~~ the extension 811 is extended in a direction of the bit line 600. Preferably, the adjacent extensions 811, between which the bit line 600 is disposed, are preferably extended in opposite directions to each other. This allows the adjacent storage electrodes to be formed on the extension 811 are arranged in a diagonal direction of the bit line 600. In addition, the adjacent extensions 811 enable the extensions 811 to be aligned with and to overlap the storage electrode. Thus, a contact resistance between the storage electrode and the storage electrode contact body 810 can be reduced.